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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,661	MATSUOKA, FUMITOMO	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-8 should be designated by a legend such as --Prior Art--, instead of the current "Background Art" label, because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are, not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 14 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Iwata et al. (U.S. Patent No. 5,880,500). With regard to Claim 14, Iwata discloses on figure 1 a semiconductor device comprising:

semiconductor substrate (100),

a first impurity diffusion layer (107) formed in the semiconductor substrate;

a second impurity diffusion layer (also 107) formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer (103a) formed on the first impurity diffusion layer;

a second insulating layer (also 103a) formed on the second impurity diffusion layer;

a trench formed, between spacers (103) and over the semiconductor substrate (100) in a manner to be defined

between the first insulting layer (103a) and the second insulating layer (also 103a);

a gate insulating film (101) lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode (102) formed as a conductive layer in the trench with the gate insulting film (101) intervening between the gate electrode conductive layer and the trench, wherein the gate electrode conductive layer is formed in an overlapped relation relative to the first impurity diffusion layer (107) and the second impurity diffusion layer (also 107).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed in figures 1-8 and described on pages 1-8 of the instant application in view of Iwata et al. (U.S. Patent No. 5,880,500). With regard to Claim 14, Applicant's admitted prior art discloses a semiconductor device comprising:

a semiconductor substrate (101),

a first impurity diffusion layer (109) formed in the semiconductor substrate;

a second impurity diffusion layer (also 109) formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer (see figure 2);

a first insulating layer (108) formed on the first impurity diffusion layer;

a second insulating layer (also 108) formed on the second impurity diffusion layer;

a trench (112) formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer (see figure 4);

a gate insulating film (201) lined on a bottom surface and an inner sidewall surface of the trench (see figure 7); and

a gate electrode (202) formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench.

Applicant's admitted prior art fails to disclose that the gate electrode conductive layer is formed in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer. However, Iwata discloses a semiconductor device, which includes a gate electrode conductive layer (102), a gate-insulating layer (101) and source/drain impurity

diffusion layers (107), which are placed in an overlapped position in relation to the gate electrode conductive layer (102) as can be seen on figure 1. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed gate electrode conductive layer formed in an overlapped relation relative to the first impurity diffusion layer and the second impurity diffusion layer, as suggested by Iwata, in order to suppress short-channel effects (column 9, lines 31-35).

With regard to Claim 15, Applicant's admitted prior art discloses a gate insulating film (201) that is formed of an insulating material having a dielectric constant of above 5 (see page 5, lines 8-16).

With regard to Claim 16, Applicant's admitted prior art discloses a gate insulating film (201) that contains one selected from the group consisting of Ta2O5, silicon nitride, A12O3, BaSrTiO3, Zr oxide, Hf oxide, Sc oxide, Y oxide, and Ti oxide (see page 4, lines 10-22 and page 5, lines 8-14).

With regard to Claim 17, Applicant's admitted prior art discloses a first impurity diffusion layer (109) and the second impurity diffusion layer (also 109), each, comprise a third impurity diffusion layer (107) including a portion formed beneath the gate insulating film formed on the inner sidewall surface of the trench (112) and a fourth impurity diffusion layer (also 107) including a portion formed beneath any of the first insulating layer (108) and second insulating

layer (also 108) and having a deeper junction in the semiconductor substrate than the third impurity diffusion layer (see page 2, lines 22-24 and figure 2).

With regard to Claim 18, Applicant's admitted prior art discloses a metal silicide layer (110) formed on the first impurity diffusion layer (109) and the second impurity diffusion layer (also 109) at those areas beneath the first insulating layer (108) and the second insulating layer (also 108), (see page 2, line 27 and page 3, lines 1-5).

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed in figures 1-8 and described on pages 1-8 of the instant application in view of Gardner (U.S. Patent No. 6,200,865). With regard to Claim 14, Applicant's admitted prior art discloses a semiconductor device comprising:

a semiconductor substrate (101),

a first impurity diffusion layer (109) formed in the semiconductor substrate;

a second impurity diffusion layer (also 109) formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer (see figure 2);

a first insulating layer (108) formed on the first impurity diffusion layer;

a second insulating layer (also 108) formed on the second impurity diffusion layer;

a trench (112) formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer (see figure 4);

a gate insulating film (201) lined on a bottom surface and an inner sidewall surface of the trench (see figure 7); and

a gate electrode (202) formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench.

Applicant's admitted prior art fails to disclose that the side edges of the gate electrode conductive layer disposed immediately above opposing edges of the first impurity diffusion layer and the second impurity diffusion layer. However, Gardner discloses on figure 6 a semiconductor device including a gate electrode conductive layer (12), spacers (22) on the sides of the gate electrode conductive layer (12), and source/drain impurity diffusion layers (24), wherein both side edges of the gate electrode conductive layer (12) are disposed immediately above opposing edges of the source/drain impurity diffusion layers (24). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed side edges of the gate electrode conductive layer disposed immediately above opposing edges of the first impurity diffusion layer and the second impurity diffusion layer, as suggested by Gardner, in order to dispose the source/drain impurity diffusion layers aligned with the edges of spacers and edges of a gate electrode conductive layer, to lower the maximum electric field developed at a drain, reduce hot-carriers effect and injection of carriers into a gate dielectric (column 6, lines 46-63).

Response to Arguments

5. Applicant's arguments with respect to claims 14-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
7/6/05

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